REMARKS

Claims 1-7, 9-27, and 29-32, and 40-43 were pending. No claims have been amended. No claims have been added or canceled. Accordingly, claims 1-7, 9-27, 29-32, and 40-43 remain pending subsequent entry of the present amendment.

Re: Examiner's Response to Arguments

In the present Office Action, claims 1-2, 4-7, 9-14, 16-17, 20-24, and 40-43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Motorola MCF5206 Integrated Microprocessor, as described in Freescale Semiconductor, Inc. Product Brief "MCF5206 Integrated Microprocessor" (hereinafter "MCF5206") and Freescale Semiconductor, Inc. "Addendum to MCF5206 User Manual" (hereinafter "MCF5206 Addendum"), in view of US Patent No. 5,025,368 (hereinafter "Watanabe") and newly cited US Patent No. 6,499,078 (hereinafter "Beckert"). Applicant has carefully considered the examiner's additional comments and believes each of the pending claims recite features that are neither disclosed nor suggested in the combination of cited art. Accordingly, Applicant traverses the above rejections and requests reconsideration.

Claim 1 recites a processing system comprising:

> "a plurality of first interrupts generated by a core, said plurality of first interrupts having programmable priorities;
> a plurality of second interrupts that are generated external to said core, said second interrupts having architecturally fixed interrupt priorities;" (emphasis added).

As stated in the Response to the Final Office Action of July 06, 2007, the features recited above in independent claim 1 are supported in the Specification as shown in the following:

> "That is, the inventor envisions that in one embodiment, the interrupts I0 through I7 should have their interrupt priority already defined (architecturally), while allowing the core interrupts to be configured as will be described further below with reference to FIG. 5." (Specification, paragraph 0040) (emphasis added)

> "For example, presume that interrupts I0-I7 have architected priorities of levels 1, 2, 3, 4, 5, 6, 7, and 8, respectively. Presume further that interrupts I8 and I9 have been programmed to have a priority level of 4.5, that interrupt I10 has a programmed priority level of 1.5, and that interrupt I11 has a programmed priority level of 0.5. Then, the encoder 440 would prioritize the received interrupts in the following order:
>
> 1 Priority Interrupt Level I11 0.5 I0 1.0 I10 1.5 I1 2.0 I2 3.0 I3 4.0 I8, I9 4.5 I4 5.0 I5 6.0 I6 7.0 I7 8.0" (Specification, paragraph 0049)

> "The present invention has thus allowed a system designer to configure an interrupt strategy for core produced interrupts without altering the interrupt priority architecture defined within an existing interrupt controller." (Specification, paragraph 0053) (emphasis added)

As can be seen above, each of the interrupts I0-I7 have one and only one architecturally fixed interrupt priority. Each of the interrupts I0-I7 have an interrupt priority defined by a system architecture and not by a user. The features of claim 1 include second interrupts having architecturally fixed interrupt priorities, which differ from priorities that are configurable. Each said second interrupt has its "interrupt priority already defined (architecturally)".

The reference MCF5206 does not teach at least these above features. MCF5206 teaches the 3 external interrupt signal lines may be configured to be used in one of two ways or modes. In the first mode, each signal is combined with the other 2 signals in order to encode an interrupt level for one interrupt. This encoding has a choice of 7 interrupt levels. In the second mode, each signal corresponds to an interrupt that may have a fixed interrupt level of 1, 4, or 7. Each interrupt is not permitted to have a value other than one of the three fixed interrupt levels (i.e. 1, 4, or 7). The term "fixed" in MCF5206 is directed to the fact that the 3 external interrupt signals may not be set to interrupt levels outside of the group of levels 1, 4, and 7. Although this group of fixed interrupt levels (i.e. 1, 4, and 7) may have interrupt level values that are architecturally defined, the 4 priority levels within each respective interrupt level is still configurable by the user. Therefore, the external interrupt signals still do not have architecturally defined priorities. There are several differences between the features of the claimed invention and MCF5206, which are discussed below.

First, regarding the second mode of use, MCF5206 nowhere discloses that any of the 3 interrupt signal lines, let alone all 3, must have one and only one interrupt level of a certain value (i.e. 1, 4, or 7). For example, MCF5206 does not disclose that the first external interrupt signal may only have interrupt level 1, the second external interrupt signal may only have interrupt level 4, and the third external interrupt signal may only have interrupt level 7. Further, their priorities would be configurable since, as disclosed by MCF5206, the 4 priority levels within the interrupt levels are configurable by the user and the interrupt levels chosen for a particular external interrupt signal may be itself configurable.

Second, MCF5206 nowhere discloses that each of the 3 external interrupt signal lines must have a different fixed interrupt level (i.e. 1, 4, or 7) from the other 2 external interrupt signals. In this case, for example, the first and second external interrupt signals may both have interrupt level 7. Again, their priorities would be configurable, rather than architecturally fixed, since the user is able to

program the first and second external interrupt signals to any one of the 4 priority levels within interrupt level 7.

Third, MCF5206 nowhere discloses the priority levels within the interrupt levels do not overlap in value. In such a case, the fixed interrupt levels (i.e. 1, 4, and 7) do not necessarily correspond to disjoint priorities. For example, if each of the 3 external interrupt signals had a separate fixed interrupt level (i.e. 1, 4, or 7), with an overlap of priority levels, the user may not be able to configure interrupt level 4 to always have a lower priority than fixed interrupt level 7. Because at least none of the above is disclosed by MCF5206, at least the highlighted features of claim 1 are not disclosed anywhere by MCF5206.

A description of the external interrupt signals of MCF5206 is provided in the following:

> "Interrupt Controller. The interrupt controller provides user-programmable control of 3 or 7 external interrupt and 5 internal peripheral interrupts . . . The 3 external interrupt signals can be configured as either fixed interrupt levels 1, 4, and 7, or as a 7-level encoded interrupt. Users can program the external interrupts to any one of the 4 priority levels within the respective interrupt levels." (MCF5206, page 5). (emphasis added).

As seen above, MCF5206 nowhere discloses the external interrupt signals have architecturally fixed priorities. In contrast, the reference explicitly states users "can program the external interrupts to any one of the 4 priority levels within the respective interrupt levels."

In the present Final Office Action, on page 18, section 44, the Examiner states:

> "When using the fixed interrupt mode of operation, the 3 external interrupts must be fixed to interrupt levels 1, 4, and 7. There is no option to fix the interrupts at other levels when using the fixed interrupt mode of operation (See 'Interrupt Controller' on Page 5). Interrupt levels 1, 4, and 7 are fixed by the architecture and cannot be programmed to other levels when using the fixed interrupt mode of operation, and thus the external interrupts have architecturally fixed interrupt priorities. This is in accordance with the definition provided by Applicant of an architecturally fixed interrupt priority: fixed by a system architecture, not configurable, and not programmable, especially by a user (See Page 9 Paragraph 2)." (emphasis added).

Claim 1 recites "second interrupts having architecturally fixed interrupt priorities". As seen in the prior discussion, MCF5206 nowhere discloses architecturally fixed priorities. Rather, MCF5206 teaches a subset of interrupt levels (i.e. 1, 4, and 7) among 7 interrupt levels may be chosen to be assigned to an external interrupt signal. Whether the 1, 4, 7, or encoded approach to interrupt levels is used, users "can program the external interrupts to any one of the 4 priority levels within the respective interrupt levels." As shown in the above discussion, MCF5206 nowhere discloses the limitations of the claimed invention.

Also in the present Office Action, the Examiner states "Applicant has acknowledged that at some stage, an architecturally fixed interrupt priority must be programmed, and that other designs in addition to hardwiring are possible". Applicant does not agree with the statement. The Examiner provides support for the above statement as follows:

> "Applicant's response dated 19 March 2006, Applicant stated (in response to the rejection that "it is unclear as to how an architecturally fixed interrupt priority can be established by an interrupt controller, as this requires some means for the interrupt priorities to be programmed") that "One skilled in the art will appreciate that such is typically accomplished based on which interrupt is physically coupled to which interrupt input

> on an interrupt controller, although other designs are possible" (See Page 10 Paragraph 2 of said response)."

Nowhere in the above does the Applicant suggest architecturally fixed interrupt priorities may be programmed by the user. Rather, architecturally fixed interrupt priorities are architected, not programmed. As shown above, assignment of priority levels may be done based on physical placement of the interrupt inputs. The above comment concerning other designs being possible refers to other means of architecting interrupt priorities. However, completely absent from the above is any statement that architected priorities may be user programmed.

In addition, as discussed in the Response to the Final Office Action of July 06, 2007, claim 1 recites a processing system comprising:

> "a priority encoder, coupled to both said first interrupts and to said second interrupts, and to said status register, said priority encoder prioritizing said first and second pluralities of interrupts utilizing said programmable priorities for said first interrupts and said architecturally fixed interrupt priorities for said second interrupts." (emphasis added)

As seen from the above, a priority encoder is recited which prioritizes programmable and architecturally fixed interrupt priorities. As already noted, the cited art does not disclose the architecturally fixed priorities as recited. Therefore, such a priority encoder is neither disclosed, inherent, nor suggested by the reference. In contrast, the reference may simply suggest a priority encoder for encoding programmable interrupt priorities. For at least these further reasons, claim 1 is patently distinguishable from the cited art.

In view of the above, Applicant submits the claims are patentably distinct from the combination of cited art. Accordingly, Applicant respectfully requests withdrawal of the rejections.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

Respectfully submitted,

/Rory D. Rankin/
Name Rory D. Rankin
Reg. No. 47,884
ATTORNEY FOR APPLICANT(S)

Date: March 18, 2008